Express Mail No. EV 346810538US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Cécil AULNETTE et al.

Application No.:

Filing Date:

For: A METHOD OF PRODUCING A SEMICONDUCTOR STRUCTURE HAVING AT LEAST ONE SUPPORT SUBSTRATE AND AN ULTRATHIN LAYER

Confirmation No.

Group Art Unit:

Examiner:

Atty. Docket No.: 4717-11900

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Pursuant to applicants' duty of disclosure under 37 C.F.R. 1.56, enclosed is a PTO form 1449 which lists (5) references for the Examiner's review and consideration.

Pursuant to the recent rule change in the Official Gazette, copies of the U.S. references are not submitted. It is respectfully requested that these references be made of record in this application by the Examiner's completion and return of the PTO Form 1449.

No fee or certification is believed to be due for the filing of this statement as it is being submitted prior to the issuance of the first office action for this application. Please charge the required fee toWinston & Strawn LLP Deposit Account No. 50-1814.

Respectfully submitted,

Date: 2/20/04

Allan A. Fanucci (Reg. No. 30,256)

WINSTON & STRAWN LLP
CUSTOMER NO. 28765
(212) 294-3311

Enclosures

LIST OF REFERENCES CITED BY APPLICANT *(Use several sheets if necessary)*	ATTY. DOCKET NO.: 4717-11900	APPLICATION SERIAL NO.:
	APPLICANT: Cecil AULNETTE et al.	
	FILING DATE: February 20, 2004	GROUP:

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	6,100,166	8/2000	Sakaguchi et al.	438	455	
	AB						
	AC						
	AD						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AE							
	AF							
	AG							

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AH	Aaron Hand, "**Value-Added Wafers Push Chips Ahead, Semiconductor International,** (2002)
	AI	M. Bruel, "**Silicon on insulator material technology**" by, "Electron Letter", 31, 1201 (1995).
	AJ	Q. Y. Tong, G. Cha, R. Gafiteau, and U. Gösele, "**Low temperature wafer direct bonding", Journal of Micro-electromechanical Systems**, 3, 29 (1994).
		Jean-Pierre Colinge, "**Silicon-On-Insulator Technology: Materials to VSLI**", 2nd Edition" by, published by "Kluwer Academic Publishers", at pages 50 and 51

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with **MPEP 609**; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.